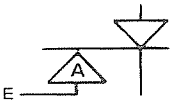
High Speed
Silicon Controlled Rectifier

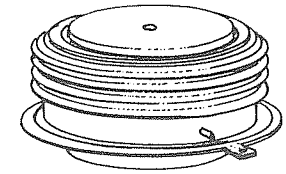
1000 A Avg. Up to 2000 Volts

C712

AMPLIFYING GATE



The General Electric device type C712 is a new pressure-mounted, high current SCR designed for power switching at high voltage and high frequencies (up to 5 KHz). The C712 gate structure has an involute, interdigitated pattern to optimize the turn-on area for high di/dt capability and it is processed using a newly developed multi-diffusion technology.



FEATURES:

- Off-State and Reverse Blocking Capabilities to 2000 Volts.
- Very Low Switching Losses at High Frequencies.
- 60 μsec Maximum Turn-Off Time at Severe Operating Conditions with Feedback diode.
- Involute, Interdigitated Gate for High di/dt Capability.
- Narrow Pulse Capability for PWM Inverter Commutating SCR Socket.
- 1″ Creepage-Path, Glazed-Ceramic Package.

IMPORTANT: Mounting instructions on the last page of C702 specification must be followed.

MAXIMUM ALLOWABLE RATINGS

TYPE	V_{DRM}/V_{RRM}[1] REPETITIVE T_J = -40°C to +125°C	V_{DRM}/V_{RRM}[1] REPETITIVE T_J = 0°C to +125°C	TRANSIENT PEAK REVERSE VOLTAGE, V_{RSM}[1] T_J = -40°C to +125°C
C712L	2000 Volts	2100 Volts	2100 Volts
C712PT	1900	2000	2000
C712PN	1800	1900	1900
C712PS	1700	1800	1800
C712PM	1600	1700	1700
C712PE	1500	1600	1600

Consult factory for lower rated voltage devices.

Peak One-Cycle Surge On-State Current, I_{TSM} (8.3 msec) . . . . 20,000 Amperes
Maximum Rate-of-Rise of Anode Current Turn-On Interval (Switching From 1200 Volts) . . . . 800 A/μsec
Repetitive di/dt Rating[2] . . . . 200 A/μsec
I^2t (for fusing) (at 8.3 milliseconds) . . . . 1,660,000 Ampere^2 Seconds
Peak Gate Power Dissipation, P_{GM} . . . . 100 Watts
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . 5 Watts
Peak Reverse Gate Voltage, V_{GRM} . . . . 20 Volts
Storage and Operating Temperature, T_{STG} and T_J . . . . -40°C to +125°C
Mounting Force Required . . . . 5000 Lb. + 1000 – 0 Lb.
22.2 KN + 4.4 – 0 KN

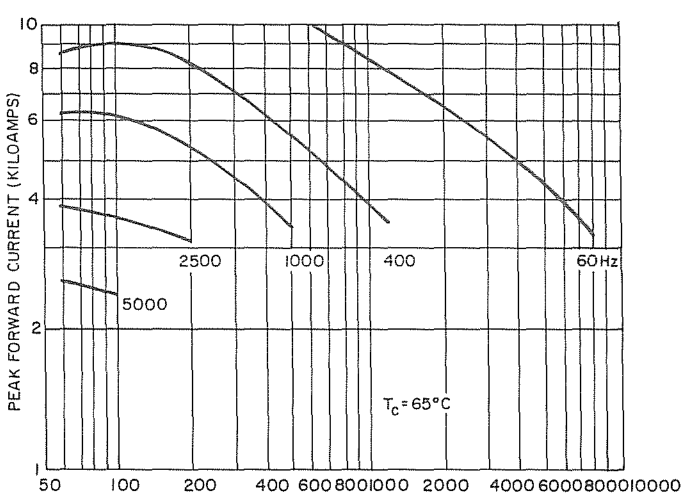
NOTES:

1 10 msec voltage sinewave.

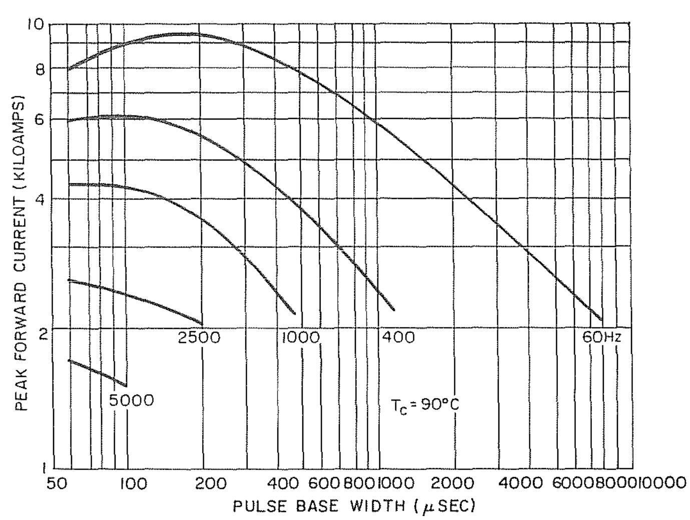
2 di/dt rating established in accordance with EIA-NEMA Standard RS-397, Section 5.2.2. This di/dt is in addition to the discharge of a 0.25 μf, 20 ohm snubber circuit in parallel with the DUT.

CHARACTERISTICS

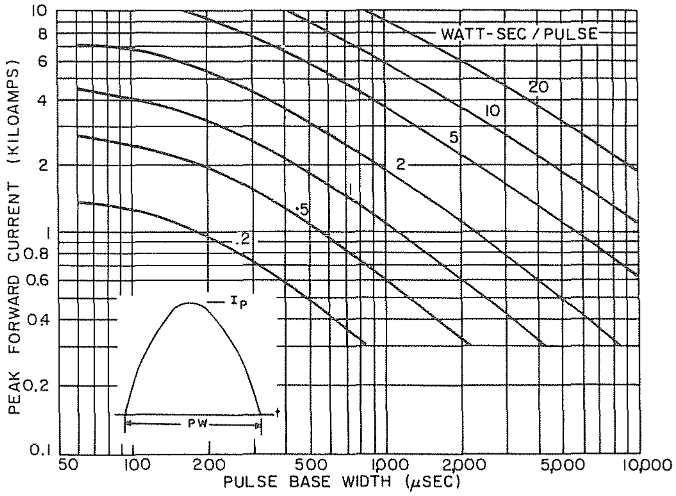
C712 TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Reverse and On-State Blocking Current	I_{DRM} and I_{RRM}	–	20	60	mA	T_J = +125°C, V = V_{DRM} = V_{RRM}
Effective Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	–	–	.023	°C/Watt	Double-Side Cooled (DC)
Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	dv/dt	500	–	–	V/μsec	T_J = +125°C, V_{DRM} = .80 Rated V_{RRM} Gate Open.
Delay Time	t_d	–	1.5	–	μsec	Switching from 140 Volts, 20 Volt, 10 Ohm Gate 0.5 μsec Rise Time, T_J = 25°C
Gate Pulse Width Necessary To Trigger		–	–	10	μsec	T_J = 25°C
Gate Trigger Current	I_{GT}	–	120	–	mAdc	T_C = 25°C, V_D = 10 Vdc, R_L = 3 Ohms
		5.0	30	–		T_C = +125°C, V_D = .5 x Rated, R_L = 1000 Ohms
Gate Trigger Voltage	V_{GT}	–	3.0	–	Vdc	T_C = 0°C to +125°C, V_D = 10 Vdc, R_L = 3 Ohms
Peak On-State Voltage	V_{TM}	–	–	1.45	Volts	T_C = +125°C, I_T = 1000 Amps. Peak Duty Cycle ⩽ 0.01%
Conventional Circuit Commutated Turn-Off Time (With Reverse Voltage)	t_q	–	–	50	μsec	(1) T_C = +125°C (2) I_T = 500 Amps. (3) V_R ⩾ 50 Volts (4) 80% V_{DRM} Reapplied (5) Rate-of-Rise of Forward Blocking Voltage = 200 V/μsec (6) Gate Bias = Open During Turn-Off Interval = 0 Volts, 100 Ohms (7) Duty Cycle ⩽ 0.01%
Conventional Circuit Commutated Turn-Off Time (With Feedback Diode)	t_q	–	55	60	μsec	(1) T_C = +125°C (2) I_T = 500 Amps. (3) V_R = 2 Volts Min. (4) 80% V_{DRM} Reapplied (5) Rate-of-Rise of Forward Blocking Voltage = 200V/μsec. (6) Gate Bias = Open During Turn-Off Interval (7) Duty Cycle ⩽ 0.01%



1. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH AT T_C = 65°C



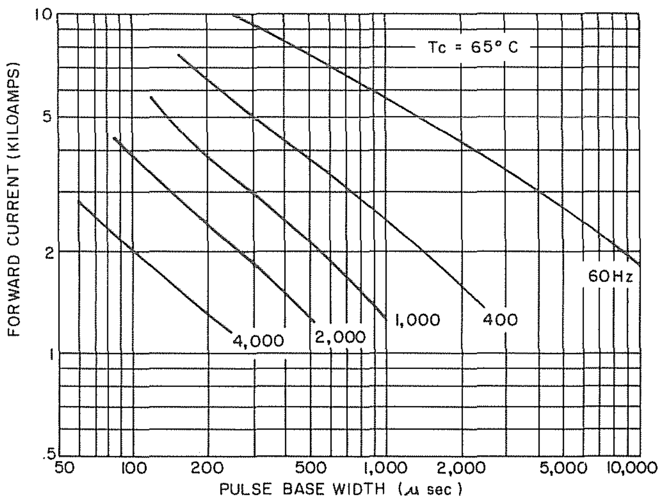
2. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH AT T_C = 90°C



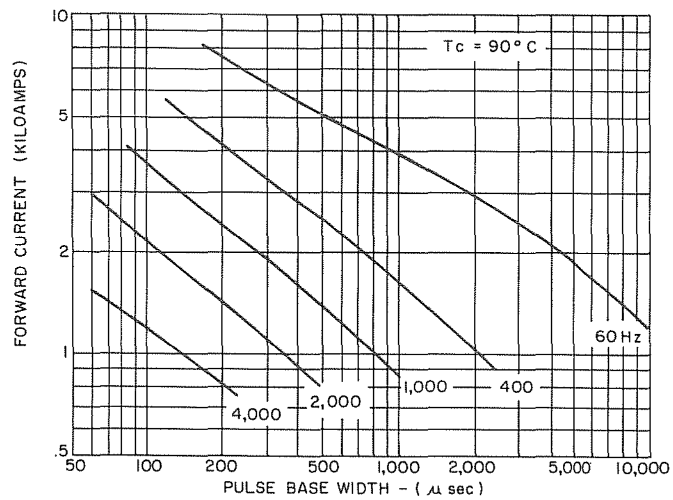
NOTES:

1. —— Switching capability and losses with bypass diode.
2. Switching voltage from 15 Volts to 0.8 V_{DRM}.
3. Snubber discharge < 50 Amps. RC time constant < 10 μsec.
4. High gate drive, 20V/10 Ohms, 0.5μsec rise time.

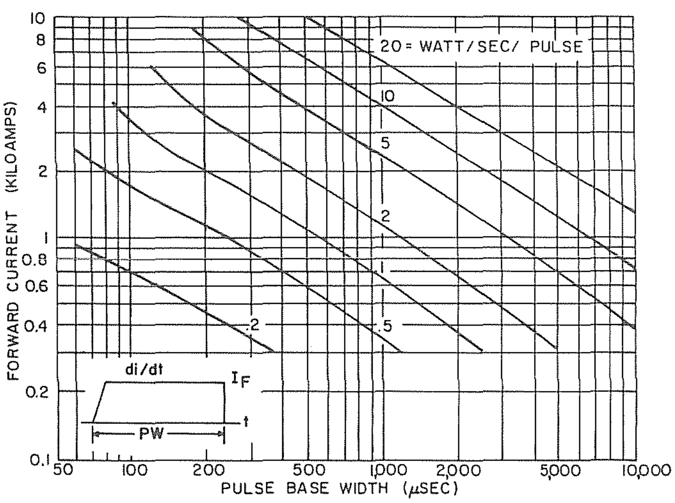
3. ENERGY PER PULSE FOR SINUSOIDAL PULSES



4. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR T_C = 65°C



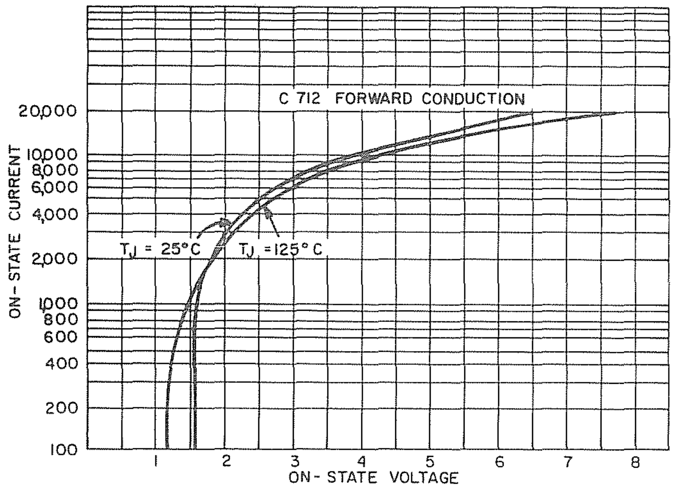
5. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR T_C = 90°C



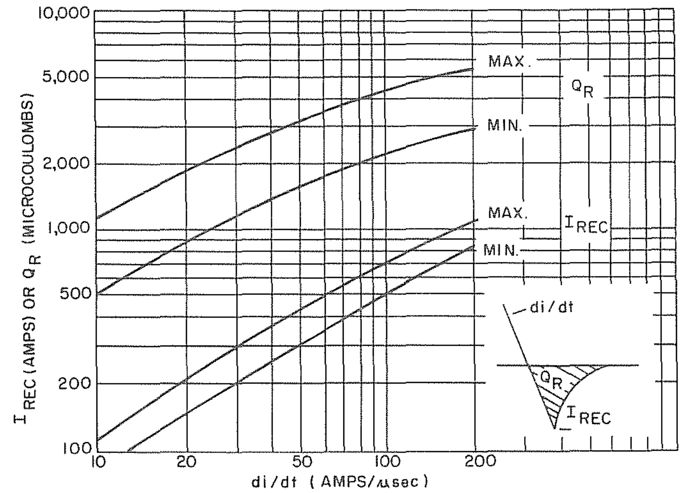
NOTES:

1. Switching voltage from 15 Volts to 0.8 V_{DRM}.
2. DI/DT during turn-on: 100A/μsec.
3 Reverse voltage < 50 Volts. If no bypass diode is used, recovery switching losses must be added.
4. RC snubber time constant < 10 μsec.
5. High gate drive: 20V/10 Ohms, 0.5μsec rise time.

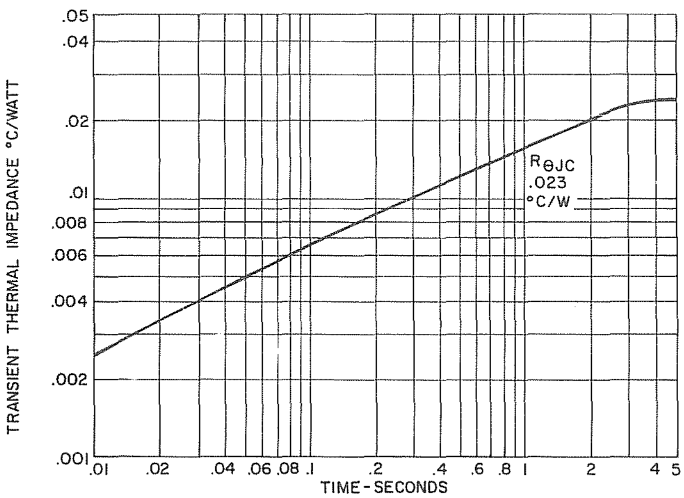
6. ENERGY PER PULSE FOR TRAPEZOIDAL CURRENT WAVEFORMS



7. FORWARD CONDUCTION CHARACTERISTIC ON-STATE



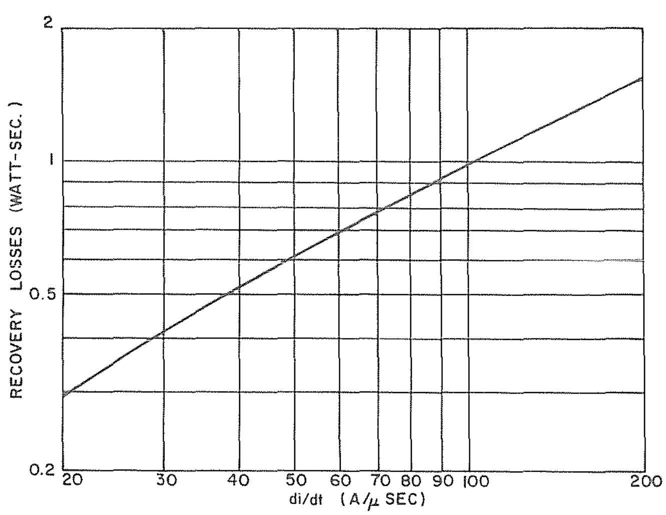
8. RECOVERED CHARGE (125°C)



NOTES:

1. Add .006°C/W to account for both case to dissipator interfaces when properly mounted; e.g., $R_{\theta JS}$ = .029° C/W. See Mounting Instructions.
2. DC Thermal Impedance is based on average full cycle junction temperature. Instantaneous junction temperature may be calculated using the following modifications:
   - end of conducting portion of cycle
     - 120° sq. wave add .0025°C/W along entire curve
     - 180° sq. wave add .0018°C/W along entire curve
     - 180° sine wave add .0010°C/W along entire curve
   - end of full cycle
     - any wave, subtract .001°C/W along entire curve

9. TRANSIENT THERMAL RESISTANCE — JUNCTION-TO-CASE



10. RECOVERY CURRENT SWITCHING LOSSES

NOTES:

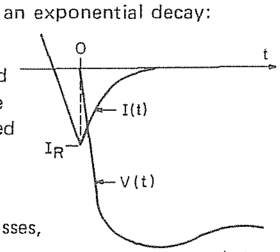
If no bypass diode is used with this thyristor, the switching losses during recovery can be significant. The actual magnitude of these losses will vary widely depending on circuit conditions and snubber design.

This curve represents typical recovery losses versus circuit di/dt. Since this curve is typical, it serves primarily to alert the equipment designer to the possible need for special design attention. The switching losses in a given circuit may be calculated with the following equation:

$$SLR = \int_0^{\infty} I(t) \cdot V(t)\ dt$$

Where SLR is the recovery switching losses; I (t) is the recovery current decay; V(t) is the recovery voltage; and t = o occurs at the peak of the recovery current. I (t) may be expressed as an exponential decay:

$$I(t) = I_R e^{-(t/T)}$$

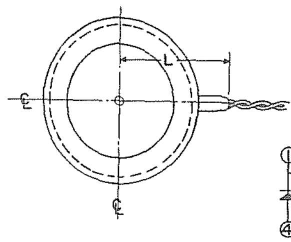


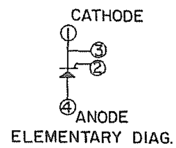
Where I_R is the peak recovery current and $T = 2.5\mu$sec. The junction temperature rise due to the recovery losses may be computed as follows:

$$\Delta T_j = F * \sigma_{\pi} * R_{\theta JA} + \alpha_{\pi} * 3.5$$

Where σ_{π} is the recovery losses, $R_{\theta JA}$ is the DC junction to ambient thermal impedance, and F is the operating frequency.

OUTLINE DRAWING





SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.200	0.240	5.08	6.10	1
φ B	0.140		3.56		
C	16.000	20.000	406.40	508.00	
φ D	1.700	1.900	43.18	48.26	
φ E		2.960		75.18	
F	1.000	1.070	25.40	27.18	
G					2.
H	.005	.067	0.13	1.70	
φ J	0.136	0.146	3.45	3.71	
K	.070		1.78		
L		2.500		63.50	
M	.030		0.76